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EXAMINER	
ROMANO, JOHN J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,496	KRISHNAN, SIVARAM	
	Examiner	Art Unit	
	John J Romano	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims **1 and 2** are rejected under 35 U.S.C. 102(e) as being clearly anticipated by **Ogawa et al,** Publication number US2002/0199177A1, (hereinafter referred to as **Ogawa**).

As per Claim **1**, **Ogawa** discloses a method for improving execution performance in a sequence of instructions that provide a function and having external access points that are external entry and external exit points, which include the steps of:

"*...determining at least one instruction, from the sequence of instructions that is necessary to be executed for less than all repetitions of the sequence of instructions; and...*" (E.g., see "Page 2, Paragraph [0017], lines 1-7);

"*modifying the sequence of instructions to isolate the one instruction from only some of the repetitions of the sequence of instructions.*" (E.g., see FIG. 2 & Page 2, Paragraph [0017], lines 7-15). **Ogawa** teaches the concept of branching around non-executable instructions not satisfying the conditional execution label or labels, thereby

isolating the one or more instructions from only the repetitions of which they do not apply.

As per Claim **2**, **Ogawa** also discloses *"...wherein said modifying includes the step of inserting at least one internal access point within the sequence of instructions and thereby partitioning the sequence of instructions into multiple segments having one of the multiple segments including the one instruction and executing for fewer times than the number of executions of another of the multiple segments."* (E.g., see FIG. 7 & Page 5, paragraph [0084], lines 1-7). **Ogawa** discloses inserting an internal label or access point, which is entered from a branch instruction, inserted by the "*branch instruction insertion unit*". Thus, thereby partitioning the sequence of instructions into multiple segments having one of the multiple segments having the one instruction executing for fewer times than the number of executions of another of the multiple segments.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim **3** is rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over **Ogawa**.

5. As per claim **3**, **Ogawa** teaches the method of claim **2** as described above. Furthermore **Ogawa** teaches *"...instructing to branch to a cycle at a top of the loop."* By branching to the beginning of the loop the step is interpreted as a recursive entry point. (E.g., see Page 2, Paragraph [0020], lines 1-12]). However, **Ogawa** does not explicitly disclose *"...wherein said inserting step inserts the one internal access point as an internal recursive entry point."*

As obvious over **Ogawa**, a person of ordinary skill in the art would have been able, at the time of the invention, to determine to include an access label after further non-executable instructions. Rather, than to have an inserted an additional branch over non-executable instructions immediately following the external entry point of the loop. In essence this involves simply moving the label to a position up or down the loop as programmers skilled in the art do on a regular basis. Thus, it would have been obvious in view of **Ogawa** to insert an internal access point as an internal recursive entry point. The motivation for doing so would have been to reduce execution instructions, which is the purpose of **Ogawa's** teachings.

6. Claims **5, 4, 6, 7, 8, 15, 16 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ogawa** as applied above, and further in view of **Subramanian**, Patent number 6,026,240, (hereinafter **Subramanian**).

7. Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ogawa** as applied to claim **2** above, and further in view of **Subramanian**. **Ogawa** discloses the method of claim **2** as disclosed above. But **Ogawa** does not expressly disclose "...*the*

step of moving the one instruction from outside of the one of the multiple segments to within the one of the multiple segments and between one of the external access points and the internal access point." However, **Subramanian** discloses an internal access point (E.g., See Fig. 5a & Col. 11, lines 4-16), where the "prologue" is the external access point and the "kernel" is the internal access point. Furthermore, **Subramanian** discloses, *"...moving the one instruction from outside of the one of the multiple segments to within the one of the multiple segments..."* (E.g., See Fig. 5b, 509 & Col. 11, lines 28-34). Where the "loop-invariant operations" are contained in the prologue, which is between the external access point and the internal access point. **Ogawa** and **Subramanian** are analogous art because they are both concerned with the same field of endeavor of optimizing programs including loops. Therefore, at the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** "omega-invariant optimizer". The motivation would be to optimize execution speed and thus improve efficiency.

8. Claim **4** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ogawa** as applied to claim **3** above, and further in view of **Subramanian** as applied to claim **5** above. **Ogawa** does not expressly disclose "...*and the internal recursive access point.*". However, **Subramanian** also discloses *"...and the internal recursive access point."* Where the "loop-invariant operations" are contained in the prologue, (E.g., See Fig. 5b & Col. 11, lines 9-13), which is between the external access point and the internal access point. Furthermore each "kernel" can be an iterative process, (E.g., See Fig. 5b & Col. 11, lines 13-21), which calls itself and therefore is an internal recursive access

point. **Ogawa** and **Subramanian** are analogous art because they are both concerned with the same field of endeavor of optimizing programs including loops. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** "omega-invariant optimizer". The motivation would be to optimize execution speed and thus improve efficiency.

9. Claim **6** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ogawa** as applied to claim **1** above, and further in view of **Subramanian**. **Ogawa** discloses the method of claim **1** as disclosed above. But **Ogawa** does not expressly disclose, "*...said modifying includes the step of rescheduling the one instruction closer in sequence of execution to one of the external access points.*". However, Subramanian discloses, "*...said modifying includes the step of rescheduling the one instruction closer in sequence of execution to one of the external access points.*" (E.g., See Fig. 5b & Col. 11, lines 29-42), where the hoisted loop-invariant instructions are executed in the prologue. It is noted that the prologue is the entry point from the external access, thereby, re-arranging or rescheduling the one instruction closer in sequence of execution to one of the external access points.

Ogawa and **Subramanian** are analogous art because they are both concerned with the same field of endeavor of optimizing programs including loops. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** "omega-invariant

optimizer". The motivation would be to optimize execution speed and thus improve efficiency.

10. In regard to claim **7**, **Ogawa** discloses the method of claim **1** as disclosed above. But **Ogawa** does not expressly disclose "*A computer readable storage media having computer readable code physically implementing a method of improving execution performance of a sequence of instructions...*". However, **Subramanian** discloses the above limitation (E.g., See Fig. 1 & Col. 8, lines 33-42), where the embodiment of the invention is a method of improving execution performance of a sequence of instructions, (E.g., See Col. 4, lines 48-57).

Ogawa and **Subramanian** are analogous art because they are both form the same field of endeavor of optimizing programs including loops. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer readable storage media", thus improving execution speed and efficiency. Thus, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions with **Ogawa's** Compiler Program.

11. In regard to claim **8**, **Ogawa** discloses the method of claim **2** as disclosed above. But **Ogawa** does not expressly disclose "A computer readable storage media having computer readable code physically implementing a method of improving execu*tion performance of a sequence of instructions...*". However, **Subramanian** discloses the above limitation (E.g., See Fig. 1 & Col. 8, lines 33-42), as stated above, where the

embodiment of the invention is a method of improving execution performance of a sequence of instructions, (E.g., See Col. 4, lines 48-57).

Ogawa and **Subramanian** are analogous art because they are both concerned with the same field of endeavor of optimizing programs including loops. Therefore, at the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer readable storage media", thus improving execution speed and efficiency. Thus, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions with **Ogawa's** Compiler Program.

12. In regard to Claim **15,** it is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ogawa** as applied to claim **3** above, and further in view of **Subramanian**. **Ogawa** discloses the method of claim **15** which includes, "*A method of machine executing a called program of a repeated sequence of instructions having at least one instruction that is necessary to be executed for less than all repetitions of the program comprising:*

...controlling at least one of said steps of executing with an internal access point other than the entry point and the exit point to isolate the one instruction within the sequence of instructions from as least one of said repeatedly calling and to execute the one instruction a number of times fewer than the total number of executions of the entire sequence of instructions." (E.g., see FIG. 2 & Page 2, Paragraph [0017], lines 1-15). **Ogawa** teaches the concept of branching around non-executable instructions not satisfying the conditional execution label or labels, thereby isolating the one or more instructions from only the repetitions of which they do not apply.

But **Ogawa** does not expressly disclose, "...*executing at least some of the sequence of instructions from an externally called entry point in the program initially;*". However, **Subramanian** discloses, "...*executing at least some of the sequence of instructions from an externally called entry point in the program initially;*" (E.g., See Fig. 5a & Col. 11, lines 4-16), where the "prologue" is the external entry point and the "kernel" is the internal access point. Furthermore, **Subramanian** discloses "...*in response to repeatedly calling, executing only some of the sequence of instructions...*" (E.g., See Fig. 5b, 509 & Col. 11, lines 28-42). Where the "loop-invariant operations" are contained in the prologue, which is between the external access point and the internal access point.

Ogawa and **Subramanian** are analogous art because they are both form the same field of endeavor of optimizing programs including loops. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** "omega-invariant optimizer". The motivation would be to optimize execution speed and thus improve efficiency.

13. In regard to claim **16**, **Ogawa** discloses the method of claim **3** as disclosed above. But **Ogawa** does not expressly disclose, "...said first-mentioned executing, includes executing the one instruction...". However, **Subramanian** discloses, "...*said first-mentioned executing, includes executing the one instruction...*" (E.g., See Fig. 5b & Col. 11, lines 29-42), as stated above, where the hoisted loop-invariant instructions are executed upon first execution, which is the prologue execution. Furthermore, **Ogawa** does not expressly disclose, "...*said second-mentioned executing recursively starts*

form the internal recursive entry point.". However, **Subramanian** discloses, "*...said second-mentioned executing recursively starts form the internal recursive entry point.* (E.g., See Fig. 5a & Col. 11, lines 4-16), where the kernel is the internal recursive entry point upon which second execution starts. Furthermore, it is interpreted that this process is executed by a CPU coupled to a memory unit as described above in claims **12, 13 and 14**, thereby being "...a method of machine executing...". It is inherent that the CPU is coupled to the memory unit, as the invention would be ineffective if not performed by a computer with a memory unit.

Ogawa and **Subramanian** are analogous art because they are both concerned with the same field of endeavor of optimizing programs including loops. Therefore, at the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer readable storage media", thus improving execution speed and efficiency. Thus, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions with **Ogawa's** Compiler Program.

14. In regard to claim **17**, claim **17** is met by the above disclosure presented in claim **16**. Claim **17** is broader in the perspective that it does not have an internal recursive entry point.

15. Claim **9** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ogawa** and **Subramanian** as applied to claim **5** above, and further in view of **Ogawa**.

16. In regard to claim **9**, **Ogawa** and **Subramanian** disclose the method of claim **5** as disclosed above. But, in claim **5**, they do not expressly disclose "...of a recursive sequence of instructions.". However, **Ogawa** discloses "...of a recursive sequence of instructions.", as discussed in claim **3** above.

17. Claim **10, 11, 12, 13, 14, 23 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ogawa** and **Subramanian** as applied to claim **6, 7, 8, and 9** above, and claim **10** below, and further in view of **Subramanian**.

18. In regard to claim **10**, **Ogawa** and **Subramanian** disclose the method of claim **6** as disclosed above. But **Ogawa** does not expressly disclose "A computer readable storage media having computer readable code physically implementing a method of improving execu*tion performance of a sequence of instructions...*". However, **Subramanian** discloses the above limitation (E.g., See Fig. 1 & Col. 8, lines 33-42), as stated above, where the embodiment of the invention is a method of improving execution performance of a sequence of instructions, (E.g., See Col. 4, lines 48-57).

Ogawa and **Subramanian** are analogous art because they are both concerned with the same field of endeavor of optimizing programs including loops. Therefore, at the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer readable storage media", thus improving execution speed and efficiency. Therefore, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions with **Ogawa's** Compiler Program.

19. In regard to claim **11**, **Ogawa** and **Subramanian** disclose the method of claim **7** as disclosed above. But in claim **7**, they do not expressly disclose "...at least one processing unit coupled to said computer readable storage media...*including at lest one volatile and non-volatile memory".* However, **Subramanian** discloses, "...at least one processing unit coupled to said computer readable storage media...", (E.g., See Fig. 1 & Col. 8, lines 33-42), where the "CPU" is interpreted as coupled to the stated "CD-ROM medium that typically contains programs". The CD-ROM medium is a non-volatile memory. Furthermore, **Subramanian** discloses "*...volatile memory*", (E.g., See Col. 14, lines 42-46). Therefore, at the time of the invention was made it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer system" to implement the method, thus improving execution speed and efficiency. Therefore, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions with **Ogawa's** Compiler Program.

20. In regard to claim **12**, **Ogawa** and **Subramanian** disclose the method of claim **8** as disclosed above. But in claim **8**, they do not expressly disclose "...at least one processing unit coupled to said computer readable storage media...*including at lest one volatile and non-volatile memory".* However, **Subramanian** discloses, "...at least one processing unit coupled to said computer readable storage media...", (E.g., See Fig. 1 & Col. 8, lines 33-42), where the "CPU" is interpreted as coupled to the stated "CD-ROM medium that typically contains programs". The CD-ROM medium is a non-volatile memory. **Subramanian** further discloses "*...volatile memory*", (E.g., See Col. 14, lines

42-46). Therefore, at the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer system" to implement the method, thus improving execution speed and efficiency. Therefore, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions with **Ogawa's** Compiler Program.

21. In regard to claim **13**, **Ogawa** and **Subramanian** disclose the method of claim **9** as disclosed above. But in claim **9**, they do not expressly disclose "...at least one processing unit coupled to said computer readable storage media...*including at lest one volatile and non-volatile memory".* However, **Subramanian** discloses, "...at least one processing unit coupled to said computer readable storage media...", (E.g., See Fig. 1 & Col. 8, lines 33-42), where the "CPU" is interpreted as coupled to the stated "CD-ROM medium that typically contains programs". The CD-ROM medium is a non-volatile memory. Furthermore, **Subramanian** discloses "*...volatile memory*", (E.g., See Col. 14, lines 42-46). Therefore, at the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer system" to implement the method, thus improving execution speed and efficiency. Thus, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions with **Ogawa's** Compiler Program.

22. In regard to claim **14**, **Ogawa** and **Subramanian** disclose the method of claim **10** as disclosed above. But in claim **10**, they do not expressly disclose "...at least one

processing unit coupled to said computer readable storage media...*including at lest one volatile and non-volatile memory".* However, **Subramanian** discloses, "...at least one processing unit coupled to said computer readable storage media...", (E.g., See Fig. 1 & Col. 8, lines 33-42), where the "CPU" is interpreted as coupled to the stated "CD-ROM medium that typically contains programs". The CD-ROM medium is a non-volatile memory. Furthermore, **Subramanian** discloses "*...volatile memory*", (E.g., See Col. 14, lines 42-46). Therefore, at the time of the invention was made it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer system" to implement the method, thus improving execution speed and efficiency. Therefore, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions with **Ogawa's** Compiler Program.

23. In regard to claims **18, 19 and 20 Ogawa** and **Subramanian** disclose the method of claim **17** as disclosed above. But in claim **17**, they do not expressly disclose "*...wherein all of said steps are included within a step of storing a program" or "..within a step of transmitting a program.", or "...within a step of receiving...".* However, **Subramanian** discloses "...at least one processing unit coupled to said computer readable storage media...", (E.g., See Fig. 1 & Col. 8, lines 33-42), where the "CPU" is interpreted as coupled to the "CD-ROM medium that typically contains programs", since a processor is required to make the program effectively operable. The CD-ROM medium is a non-volatile memory. Furthermore, **Subramanian** discloses "*...volatile memory*", (E.g., See Col. 14, lines 42-46). In either case, the act of the CPU executing

an instruction to store the program from volatile to non-volatile memory is well known by those in the programming art. Thus, meeting the further limitation of "...*wherein all of said steps are included within a step of storing a program" or "...within transmitting a program", or "...receiving the program.",* the data of the program instructions being transmitted via the data-bus via direction from the CPU and furthermore, the act of the memory receiving the program from the data-bus. Therefore, at the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer system" to implement the method, thus improving execution speed and efficiency. Thus, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions via a computer system with **Ogawa's** Compiler Program.

24. In regard to claims **21 and 22**, **Ogawa** and **Subramanian** disclose the method of claim **17** as disclosed above in claim **17**. But in claim **17**, they do not expressly disclose "...*wherein all of said steps are included with a step of executing a program or "...wherein all of said steps are included within a step of machine modifying a program.*". However, **Subramanian** additionally discloses the above limitations, (E.g., See Col. 14, lines 42-46). In either case, the act of the CPU executing an instruction to compile the program from volatile or non-volatile memory is well known by those in the programming art as modifying, (via compiling), and executing the program, (performing the steps of the process via CPU). Thus, meeting the further limitation of "...*wherein all of said steps are included within a step of executing a program", or "...within a step of*

machine modifying a program.". Therefore, at the time of the invention was made it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer system" to implement the method, thus improving execution speed and efficiency. Therefore, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions via a computer system with **Ogawa's** Compiler Program.

25. In regard to claim **23**, **Ogawa** and **Subramanian** disclose the method of claim **6** as disclosed above. But **Ogawa** does not expressly disclose "...comprising a storage media;...". However, **Subramanian** discloses "...comprising a storage media;...", (E.g., See Fig. 1 & Col. 8, lines 33-42), as stated above, where the CD-ROM medium is a storage media.

Ogawa and **Subramanian** are analogous art because they are both concerned with the same field of endeavor of optimizing programs including loops. Therefore, at the time of the invention was made it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer readable storage media", thus improving execution speed and efficiency. Therefore, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions with **Ogawa's** Compiler Program.

26. In regard to claim **24**, **Ogawa** and **Subramanian** disclose the method of claim **23** as disclosed above. But **Ogawa and Subramanian** do not expressly disclose "...said means for rescheduling providing internal recursive access between an entry point and an exit point of the sequence of instructions...". *However,* **Subramanian** further

discloses "...said means for rescheduling providing internal recursive access between an entry point and an exit point of the sequence of instructions...", (E.g., See Fig. 5b & Col. 11, lines 29-42), where the hoisted loop-invariant instructions are executed in the prologue. It is noted that the prologue is the entry point from the external access, thereby, re-arranging or rescheduling the one instruction closer in sequence of execution to one of the external access points.

Ogawa and **Subramanian** are analogous art because they are both concerned with the same field of endeavor of optimizing programs including loops. Therefore, at the time of the invention was made it would have been obvious to a person of ordinary skill in the art to modify **Ogawa's** compiler with **Subramanian's** teachings of a "computer readable storage media", thus improving execution speed and efficiency. Therefore, it would have been obvious to combine **Subramanian's** method of improving execution performance of a sequence of instructions with **Ogawa's** Compiler Program.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Odani et al, Patent No. US 6,243,864 B1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J Romano whose telephone number is (703) 305-0358. The examiner can normally be reached on 8-5:30, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***

TUAN DAM
SUPERVISORY PATENT EXAMINER